WHAT IS CLAIMED IS:

1. An apparatus for DBWRR (Delay Bound Weighted Round Robin) cell scheduling in an ATM (Asynchronous Transfer Mode) switch, comprising:

a plurality of input buffers, each of said input buffers storing high-speed ATM cell groups in order;

a queuing module for receiving high-speed ATM cells, grouping the received ATM cells according to scheduling cycles on a link basis and storing the resulting ATM cell groups in said input buffers;

a plurality of ATM cell scheduling tables for storing and managing cell scheduling information about said ATM cell groups stored in corresponding ones of said input buffers;

an ATM processor for processing and transferring said ATM cell groups stored in each of said input buffers on the basis of the cell scheduling information in each of said ATM cell scheduling tables, a preset weight, a delay time required by an earliest cell in a first one of said ATM cell groups stored in each of said input buffers and an allowable delay time required by each of said input buffers;

a multiplexer connected in common to said input buffers for inputting a plurality of ATM cells from said input buffers and providing the inputted ATM cells as a single output signal; and

an output buffer for inputting an ATM cell signal from said multiplexer and temporarily storing the inputted ATM cell signal for an output wait period of time.

2. The apparatus as set forth in claim 1, wherein each of said ATM cell scheduling tables includes a plurality of ATM cell scheduling storage sections, each of said ATM cell scheduling storage sections storing and managing said cell scheduling information about an associated one of said ATM cell groups stored in a corresponding one of said input buffers.

3. The apparatus as set forth in claim 2, wherein each of said ATM cell scheduling storage sections includes:

an index region for storing an index of a corresponding one of said ATM cell scheduling storage sections;

a cell number region for storing the number of ATM cells in the associated ATM cell group stored in the corresponding input buffer;

an allowable cycle region for storing a number of an allowable cycle of said associated ATM cell group stored in said corresponding input buffer; and

a reserved counter region for storing a reserved counter value of said associated ATM cell group stored in said corresponding input buffer.

4. The apparatus as set forth in claim 1, wherein said ATM processor is adapted to, if said delay time required by said earliest cell in said first ATM cell group stored in each of said input buffers is less than or equal to said allowable delay time required by each of said input buffers, the number of cells in said first cell group is greater than said weight and an allowable cycle of said first cell group is not "0", transfer the same number of cells in said first cell group as said weight to said output buffer via said multiplexer.

5. The apparatus as set forth in claim 1, wherein said ATM processor is adapted to, if the number of cells in said first cell group stored in each of said input buffers is greater than said weight and an allowable cycle of said first cell group is "0", transfer the same number of cells in said first cell group as "said weight + a reserved counter value indicative of arrival of a first cell of said first cell group" to said output buffer via said multiplexer.

6. The apparatus as set forth in claim 4, wherein said ATM processor is adapted to, if the number of cells in said first cell group stored in each of said input buffers is smaller than or equal to said weight, transfer all cells in said first cell group and then the same number of cells in a second one of said ATM cell groups stored in each of said input

buffers as a remainder of said weight to said output buffer via said multiplexer.

7. The apparatus as set forth in claim 4, wherein said ATM processor is adapted to, if said delay time required by said earliest cell in said first ATM cell group stored in each of said input buffers is greater than said allowable delay time required by each of said input buffers, the number of cells in a second one of said ATM cell groups stored in each of said input buffers is greater than said weight and an allowable cycle of said second cell group is not "0", discard all cells in said first cell group and transfer the same number of cells in said second cell group as said weight to said output buffer via said multiplexer.

8. The apparatus as set forth in claim 4, wherein said ATM processor is adapted to, if said delay time required by said earliest cell in said first ATM cell group stored in each of said input buffers is greater than said allowable delay time required by each of said input buffers, the number of cells in a second one of said ATM cell groups stored in each of said input buffers is greater than said weight and an allowable cycle of said second cell group is "0", discard all cells in said first cell group and transfer the same number of cells in said second cell group as "said weight + a reserved counter

value indicative of arrival of a first cell of said second cell group" to said output buffer via said multiplexer.

9. The apparatus as set forth in claim 4, wherein said ATM processor is adapted to, if said delay time required by said earliest cell in said first ATM cell group stored in each of said input buffers is greater than said allowable delay time required by each of said input buffers and the number of cells in a second one of said ATM cell groups stored in each of said input buffers is smaller than or equal to said weight, discard all cells in said first cell group and transfer all cells in said second cell group and then the same number of cells in a third one of said ATM cell groups stored in each of said input buffers as a remainder of said weight to said output buffer via said multiplexer.

10. A method for DBWRR (Delay Bound Weighted Round Robin) cell scheduling in an ATM (Asynchronous Transfer Mode) switch, comprising the steps of:

(a) allowing a queuing module to receive high-speed ATM cells, group the received ATM cells according to scheduling cycles on a link basis and store the resulting ATM cell groups in a specific one of a plurality of input buffers;

(b) allowing an ATM processor to store cell scheduling information about said ATM cell groups stored in the specific

input buffer, in a specific one of a plurality of ATM cell scheduling tables, corresponding to said specific input buffer;

(c) allowing said ATM processor to recognize the cell scheduling information about a first one of said ATM cell groups stored in said specific input buffer, from said specific ATM cell scheduling table;

(d) allowing said ATM processor to calculate a delay time required by an earliest cell in said first ATM cell group stored in said specific input buffer and an allowable delay time required by said specific input buffer;

(e) allowing said ATM processor to determine how to process cell transfer scheduling for said first cell group stored in said specific input buffer on the basis of said ATM cell scheduling information about said first cell group stored in said specific ATM cell scheduling table, said delay time required by said earliest cell in said first cell group and said allowable delay time required by said specific input buffer, and then process the cell transfer scheduling for said first cell group in accordance with the determination result; and

(f) allowing said ATM processor to update said ATM cell scheduling information about said first cell group stored in said specific ATM cell scheduling table in such a manner that it is appropriate to a current cell group transfer process.

11. The method as set forth in claim 10, wherein said cell scheduling information about said ATM cell groups includes the number of cells and an allowable cycle of each of said ATM cell groups, and a reserved counter value indicative of arrival of a first cell of each of said ATM cell groups.

12. The method as set forth in claim 10, further comprising the step of:

(g) allowing said ATM processor to, if it is determined at said step (e) that said delay time required by said earliest cell in said first ATM cell group stored in said specific input buffer is less than or equal to said allowable delay time required by said specific input buffer, the number of cells in said first cell group is greater than a weight and an allowable cycle of said first cell group is not "0", transfer the same number of cells in said first cell group as said weight to an output buffer via a multiplexer.

13. The method as set forth in claim 10, further comprising the step of:

(g) allowing said ATM processor to, if it is determined at said step (e) that the number of cells in said first cell group stored in said specific input buffer is greater than a weight and an allowable cycle of said first cell group is "0", transfer the same number of cells in said first cell group as

"said weight + a reserved counter value indicative of arrival of a first cell of said first cell group" to an output buffer via a multiplexer.

14. The method as set forth in claim 10, further comprising the step of:

(g) allowing said ATM processor to, if it is determined at said step (e) that the number of cells in said first cell group stored in said specific input buffer is smaller than or equal to a weight, transfer all cells in said first cell group and then the same number of cells in a second one of said ATM cell groups stored in said specific input buffer as a remainder of said weight to an output buffer via a multiplexer.

15. The method as set forth in claim 10, further comprising the step of:

(g) allowing said ATM processor to, if it is determined at said step (e) that said delay time required by said earliest cell in said first ATM cell group stored in said specific input buffer is greater than said allowable delay time required by said specific input buffer, the number of cells in a second one of said ATM cell groups stored in said specific input buffer is greater than a weight and an allowable cycle of said second cell group is not "0", discard all cells in said first cell group and transfer the same number of cells in said second cell

group as said weight to an output buffer via a multiplexer.

16. The method as set forth in claim 10, further comprising the step of:

(g) allowing said ATM processor to, if it is determined at said step (e) that said delay time required by said earliest cell in said first ATM cell group stored in said specific input buffer is greater than said allowable delay time required by said specific input buffer, the number of cells in a second one of said ATM cell groups stored in said specific input buffer is greater than a weight and an allowable cycle of said second cell group is "0", discard all cells in said first cell group and transfer the same number of cells in said second cell group as "said weight + a reserved counter value indicative of arrival of a first cell of said second cell group" to an output buffer via a multiplexer.

17. The method as set forth in claim 10, further comprising the step of:

(g) allowing said ATM processor to, if it is determined at said step (e) that said delay time required by said earliest cell in said first ATM cell group stored in said specific input buffer is greater than said allowable delay time required by said specific input buffer and the number of cells in a second one of said ATM cell groups stored in said specific input

buffer is smaller than or equal to a weight, discard all cells in said first cell group and transfer all cells in said second cell group and then the same number of cells in a third one of said ATM cell groups stored in said specific input buffer as a remainder of said weight to an output buffer via a multiplexer.

18. The method as set forth in claim 10, wherein said step (d) includes the step of allowing said ATM processor to calculate said delay time required by said earliest cell in said first ATM cell group stored in said specific input buffer on the basis of the below equation:

$$QD' = (k - c_1)W - (RC - RC_1)$$

where, k is a period in which cells in each ATM cell group must be processed, c_1 is an allowable cycle of a cell group being currently serviced, W is time (10δ) required in processing cells associated with weights of all input buffers, RC is a reserved counter value when each ATM cell group has arrived at a corresponding input buffer, and RC_1 is a reserved counter value when a first cell of each ATM cell group has arrived at a corresponding input buffer.

19. The method as set forth in claim 10, wherein said step (d) includes the step of allowing said ATM processor to calculate said allowable delay time required by said specific

input buffer on the basis of the below equation:

$$D_t = kW + \alpha \qquad (0 \le \alpha \le W)$$

where, k is a period in which cells in each ATM cell group must be processed, and W is time (10δ) required in processing cells associated with weights of all input buffers.